HIGH DENSITY MICROWAVE PACKAGING FOR T/R MODULES

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ABSTRACT

This paper describes the development of low cost 3-D packaging of transmit/receive (T/R) modules for an active array radar at X-band. The development focused on the design, manufacture and interconnection of multi-layer aluminum nitride (AlN) substrates. The substrates are electrically joined together with solderless interconnects. All GaAs and most silicon chips have been flipped for achieving low cost assembly and higher reliability. The major microwave transmission line is conductor backed coplanar line CBCPW which interfaces with the coplanar line used on the flipped microwave chip. The interconnect technology is applicable to commercial high speed data lines that are concerned about preserving the fast rise time of the signal.

Introduction

The T/R module is the major cost driver of an active array. It represents at least fifty percent of the overall array cost. In addition the package geometry chosen for the module has an enormous leverage effect on the cost and weight of other supporting elements of the array. The supporting elements most affected are the signal manifolds and the liquid cooling which are electrically and mechanically attached respectively to the module. A new high density microwave package has the potential for reducing the module cost, weight, and depth and also that of the supporting elements. This paper will focus on a high density module development that uses 3-D packaging. This module resembles a tile since it is approximately 1 inch square by 0.3 inches thick. Because of the large surface area at the ends of the module, both electrical and mechanical connection can be made simultaneously to the active array. This feature will reduce array fabrication and assembly costs. Figure 1 shows the tile like module and the three multilayer AlN substrates that are electrically joined together to produce four T/R elements. The weight of each element is about 20 percent of a conventional module.

Microwave Interconnects

For ease of assembly, disassembly of the prototype development of the 3-D package, we choose to use solderless fuzz buttons and the elastomeric connector metal on elastomer (MOE). For 3-D packaging, a major requirement is the determination of the alignment tolerance of microwave signal pads between layers that use solderless interconnects. This is an extremely tedious and time consuming task to make these measurements manually. A computer controlled optical bench was adapted to precisely measure x and y displacements between signal pads on adjoining substrate layers. Figure 2a and b show a block diagram of the automatic vertical interconnect station (AVITS) and the test fixture for an elastomeric interconnect between two substrates using CBCPW. This AVITS machine saved many hours and helped determine alignment tolerances for both the fuzz and the MOE connectors.

In order to design the 3-D package for the module, all possible microwave interconnects were modeled using the high frequency structure simulation tool HFSS. All the potential interconnects were then fabricated in AlN and measured experimentally. Quite often the results did not agree with the simulations because the manufactured geometry was not precisely the same as the model. The measured data was used to design and predict the performance of the module. Our first design used all elastomeric interconnects between the three AlN substrates.

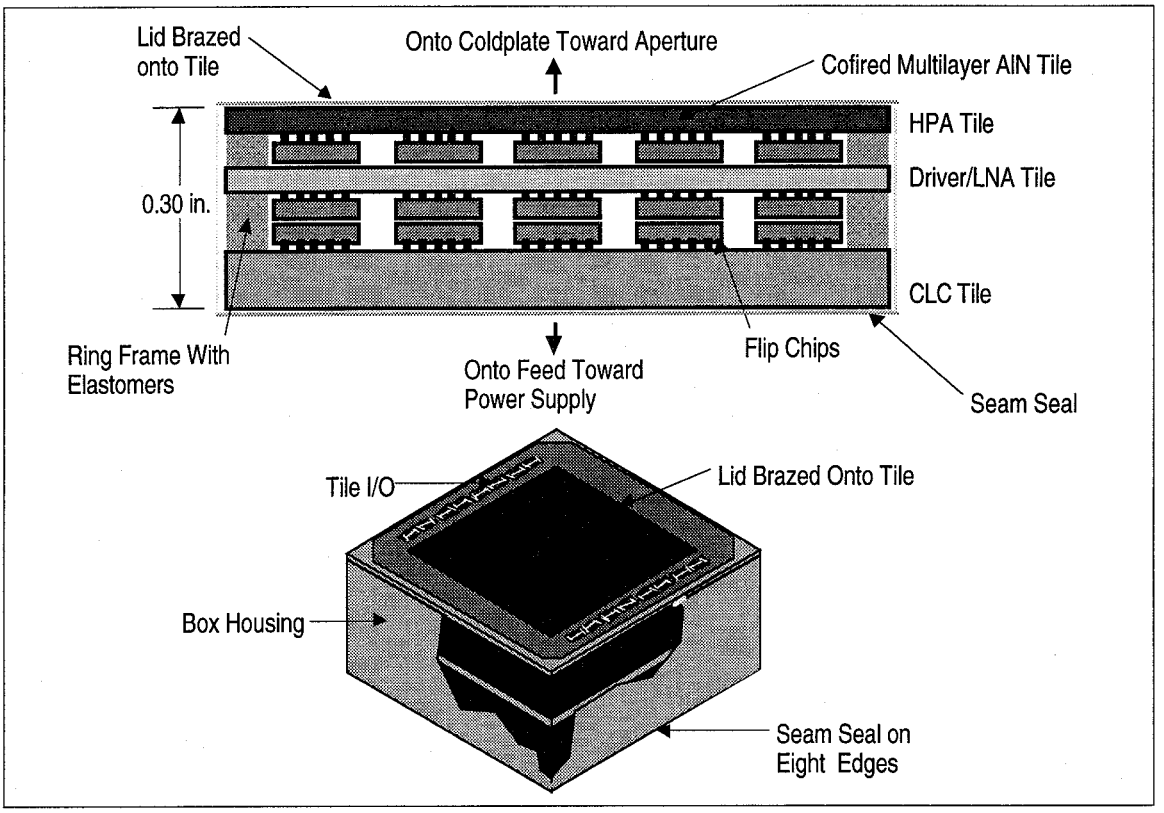

Figure 1. 3-D Packaging for the T/R Module. The module contains four T/R elements that are packaged in a volume of 0.3 cubic inches and weighs less than one ounce.

Multilayer Substrate Design

The T/R module uses both silicon and GaAs chips. The GaAs chips produce approximately 32 watts of cw microwave power within the package and are 20 to 30 percent efficient. Hence AlN was selected for good thermal conductivity and CTE match to both silicon and GaAs. In order to ensure good alignment between signal lines on adjoining substrates, we selected a hot pressed AlN sintering process that guaranteed excellent xy registration (± 1 to 2 mils). This hot pressed technology was manufactured by Coors in Chatanooga, Tennessee. The thickness of the substrate was determined by the separation between ground and the CPW and stripline transmission lines. The AlN layers are approximately 5 mils thick, and the electrical designer was able to route all the other required signal lines on the intervening layers. Keepout regions were required directly below the microwave transmission lines.

Package Design

For a three layer stack of substrates, the middle layer must have a good thermal path to the outside of the package. This path is provided by aluminum ring frames that hold the elastomeric connectors in place. Since the connectors are not rigidly attached to the substrates there is no need to match the CTE of the ring frame to the AlN. Contact of the ring frames with the AlN substrates provide a sufficient heat path so that the flipped GaAs chips operate below 100 degrees centrigrade. We have calculated and measured that the flipped chips with thermal bumps on the sources of the FETs provide a better thermal conduction than a 4 mil thinned unflipped chip. All of these thermal calculations were performed with the software CINDA and measured with a Barnes Computherm. The three substrates and the elastomeric conductors and ring frames are contained within a kovar sleeve that is seam sealed to kovar end rings. The end rings had been brazed onto the outside surface of the AlN substrates during their manufacture at Coors. We

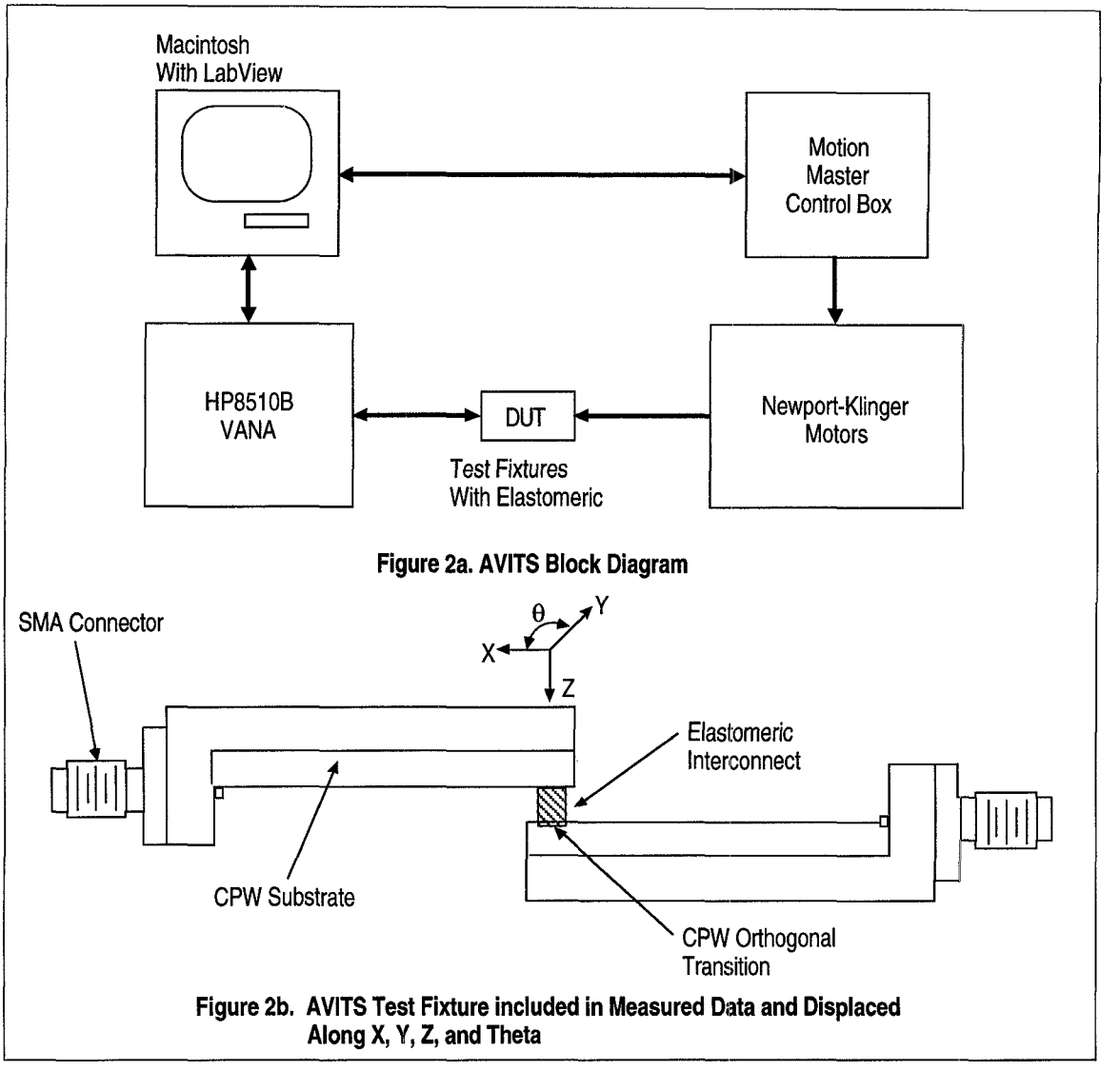

Figure 2. Automatic Vertical Interconnect Test System (AVITS). The instrument was used to determine xy displacement tolerances between microwave signal lines on adjoining substrates.

have subjected the package to approximately 800 thermal cycles from minus 125°C to plus 100°C with no degradation of the hermeticity.

Advantages of the HDMP Module

The module shown above can be readily manufactured on a conventional substrate assembly line. No new tools or processes are required. As mentioned previously, module weight is reduced by 80 percent over a conventional module. We have assembled several modules at HE Microwave and they have estimated assembly costs compared to a conventional type. Figure 3 shows the projected assembly costs relative to the older design. The figure shows that assembly costs are reduced by about 65 percent. The module has been designed so that the HPAs are all on one substrate. As the design of the HPA changes towards higher powers, efficiency and bandwidth, only one substrate will require redesign. The module is presently being tested at Hughes and preliminary test results will be available at Orlando.

The author wishes to thank all the Hughes employees that contributed to the design, assembly and test of this module. In addition the program was supported by an ARPA, tri service contract number F33615-93-C-1292.

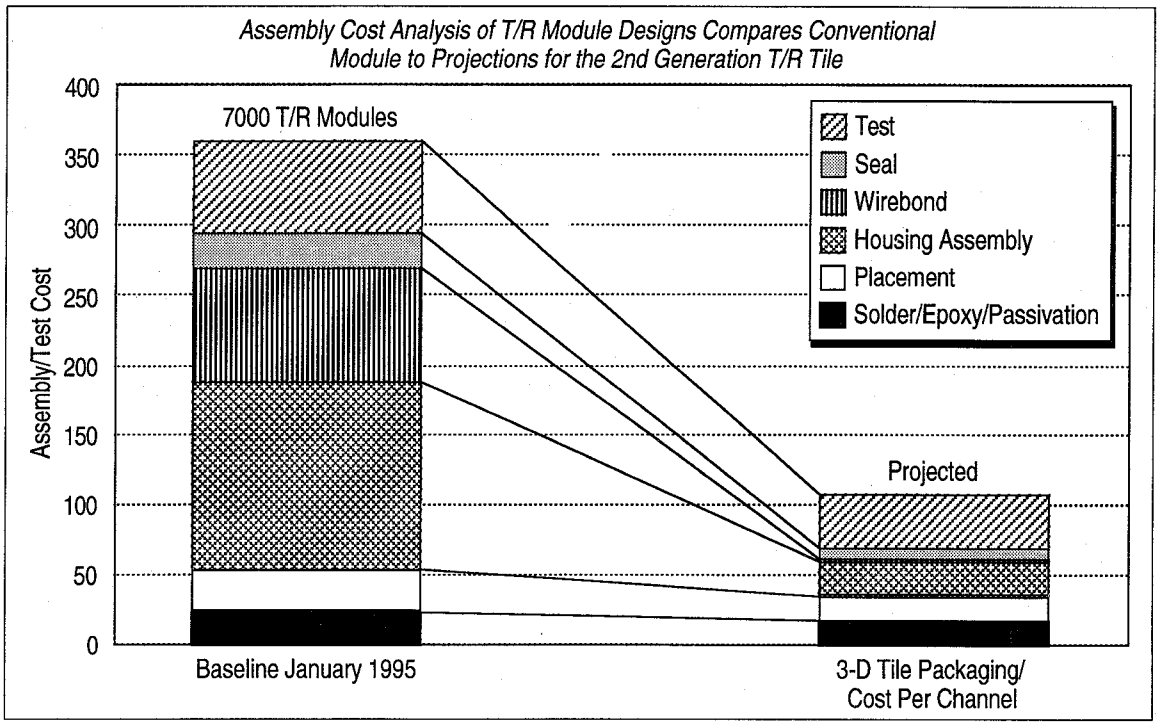

Figure 3. Assembly Cost Analysis of T/R Module Design. The first generation tile design is estimated to reduce the production assembly cost by nearly two-thirds.